REMARKS

The Office Action dated February 2, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 2, 4-6, 12, 14-16, and 21 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1, 2 and 4-21 are pending in the present application and are respectfully submitted for consideration.

Claims 1, 2, 4, 5, and 16-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takahashi et al. (JP 40927070, "Takahashi") in view of Volk et al. (U.S. Patent No. 5,999,020, "Volk"). Applicant respectfully submits that each of claims 1, 2, 4, 5 and 16-21 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites an input circuit comprising a current mirror circuit including a self-biased transistor and a non-self-biased transistor connected to each other, a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal, wherein a first source of the first transistor and a second source of the second transistor are connected in common and have the same potential, and the differential circuit generates a node signal having a rising edge and a falling edge at the first drain

in accordance with a current flowing through the first and second transistors, a constant current source connected to the first source of the first transistor, and a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source, wherein the current regulating circuit increases an amount of the current flowing through the differential circuit in response to the node such that only a rising delay time of the node signal is shortened.

Claim 16 recites an input circuit comprising a first MOS transistor having a gate that receives a data signal, a second MOS transistor having a gate connected to a reference voltage, wherein the source of the first transistor is connected to the source of the second transistor at a first node, a third MOS transistor connected between the first node and a low potential power supply, and having its gate connected to a high potential power supply, a fourth MOS transistor connected between the first node and the low potential power supply, a fifth MOS transistor connected between the drain of the first transistor and the high potential power supply, a sixth MOS transistor connected between the drain of the second transistor and the high potential power supply, wherein the gates of the fifth and sixth transistors are connected to each other and to the drain of the sixth transistor, and a first inverter haring an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, wherein a node signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors, and wherein the fourth transistor operates to increase the amount of

the current flowing through the second transistor in response to the node signal such that only a rising delay time of the node signal is shortened.

Accordingly, at least one of the essential features of the present invention is a differential circuit that generates a node signal having a rising edge and a falling edge at the first drain in accordance with a current flowing through a first and a second transistors with respect to claim 1; and a node signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors, and wherein the fourth transistor operates to increase the amount of the current flowing through the second transistor in response to the node signal such that only a rising delay time of the node signal is shortened, with respect to claim 16. As such, the present invention results in the advantage of having an input circuit generating internal input node signal which rise and fall in response to the rising edges and the falling edges of an external input signal.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention as set forth in claims 1, 2, 4, 5 and 16-21, and therefore fails to provide the advantages which are provided by the present application.

Applicant respectfully submits that each and every element recited within claims 1 and 16 is neither disclosed nor suggested by Takahashi or Volk, taken together or in combination. In particular, Applicant submits that the input circuit as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the limiting element of "the differential circuit generates a node signal

having a rising edge and a falling edge at the first drain in accordance with a current flowing through the first and second transistors" and "a node signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors, and wherein the fourth transistor operates to increase the amount of the current flowing through the second transistor in response to the node signal such that only a rising delay time of the node signal is shortened".

Applicant submits that Takahashi merely discloses a transistor (P2 or N6). The Examiner took the position that the transistor (P2 or N6) of Takahashi reads on a current adjustment transistor for receiving a differential output signal via a three stage inverter (DL1 or DL2). However, it is submitted that Takahashi does not teach or suggest that the transistor (P2 or N6) increases the amount of the current flowing through the differential circuit in response to a node signal such that only a rising delay time of the node signal is shortened. In other words, since the transistor (N6) of is turned off when a node signal (N4; Fig. 4) is rising, it is not possible to increase the amount of a current through the differential circuit to shorten a rising delay time of the node signal (N4).

In addition, Volk merely discloses an input buffer that includes transistors (30, 32) for increasing the amount of the current flowing through the differential circuit (54, 62) in response to an output signal (28). However, Applicant submits that Volk does not disclose that only a rising delay time of the node signal is shortened when responding to a node signal. Volk shows the quick rise and fall of a node signal at a node between the transistors (54, 58) using the transistors (30, 32). Accordingly, Volk does not obtain

a differential output signal in which a failing delay time and a rising delay time of the differential output signal are substantially the same (see Figs. 3 and 7 of the present specification).

Consequently, Applicant submits that neither Takahashi nor Volk, disclose or suggest each and every element of claim 1 and claim 16 of the present application, and therefore claims 1 and 16 are allowable.

Claims 6-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fig. 1 of Applicant's admitted prior art ("AAPA") in view of Takahashi and further in view of Volk. Applicant respectfully submits that each of claims 6-20 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 6 recites a semiconductor integrated circuit comprising a plurality of input circuits. Each input circuit includes a differential circuit including a first transistor for receiving an external signal and a second transistor for receiving a reference signal, wherein sources of the first and second transistors are connected in common, and the differential circuit generates a node signal having a rising edge and a failing edge at a drain of the first transistor in accordance with a current flowing through the first and second transistors, and a current regulating circuit, connected to the differential circuit, which increases the amount of the current flowing through the differential circuit in response to the node signal such that only a rising delay time of the node signal is shortened, a plurality of complementary signal generating circuits, each connected to one of the input circuits, wherein the complementary signal generating circuits receive the node signal from the associated input circuit and generate a complementary signal

of the input signal, and a plurality of signal processing circuits connected to the plurality of complementary signal generating circuits, respectively, wherein the signal processing circuits perform predetermined signal processing operations in accordance with the complementary signal.

Figure 1 of AAPA merely discloses an input latch circuit having a first input circuit, a second input circuit, and a latch circuit. The first input circuit receives an external data strobe signal DQS through an input pad.

Applicant further submits that neither Takahashi nor Volk discloses the fourth transistor of the present invention that operates to increase the amount of the current flowing through the second transistor in response to the node signal such that only a rising delay time of the node signal is shortened. Accordingly, the invention of claims 6 and 16 is not obvious over Takahashi in view of Volk and is not obvious over Fig. 1 of the Applicant's admitted prior art in view of Takahashi and further in view of Volk.

As for claims 7-15 and 17-20, it is submitted that each of these claims is dependent on independent claims 6 and 16, respectively. As such, each of claims 7-15 and 17-20 is allowable due to its dependency on allowable claims 6 and 16, respectively.

In view of the above, Applicants respectfully submit that each of claims 1, 2, 4-21 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully

request that claims 1, 2, and 4-21 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108075-09014.

Respectfully submitted,

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